--[0003.1] The present invention provides a data transmission system for serial asynchronous data transmission between a first unit and a second unit. The data transmission system includes a first circuit part associated with the first unit and a second circuit part associated with the second unit. The first circuit part includesa first transmitter circuit part including a first transmitter terminal; a first receiver circuit part including a first receiver terminal; a first terminal for a data transmission line; and a first terminal for a reference potential line. The second circuit part includes a second transmitter circuit part including a second transmitter terminal; a second receiver circuit part including a second receiver terminal; a second terminal for the data transmission line; and a second terminal for the reference potential line. The second circuit part is interconnectable with the first circuit part via the data transmission line for bidirectional data transmission and via the reference potential line. A current source is provided which is configured for feeding a current into the data transmission line so that a first signal state of the first receiver terminal is capable of being changed as a function of a second signal state of the second transmitter terminal; and a third signal state of the second receiver terminal is capable of being changed as a function of a fourth signal state of the first transmitter terminal--.

Please delete paragraph [0004].

Please amend paragraph [0005] as follows:

[0005] The power supply to the circuit part, which may be galvanically separated, of the first device, which may be a master device, via the bus side is ensured according to the present invention by feeding a current, in particular a constant current, into the single, bidirectional data transmission line of the system.

Before paragraph [0009], please insert the heading --BRIEF DESCRIPTION OF THE DRAWINGS--.

Please amend paragraph [0009] as follows:

[0009] Further details and advantages of the present invention will be elaborated upon below based on exemplary embodiments with reference to the drawings, in which:

Please amend paragraph [0010] as follows:

[0010] Figure 1 shows a schematic representation of a data transmission system according to the present invention;

Figure 2: shows a schematic representation of an embodiment of a data transmission system according to Fig. 1; and

Figure 3 shows a schematic representation of a data transmission system according to another embodiment of the present invention.

Before paragraph [0011], please insert the heading --DETAILED DESCRIPTION--.

Please amend paragraph [0011] as follows:

[0011] According to Fig. 1, a data transmission system according to the present invention includes two circuit parts which can be interconnected via a two-pole line 8.

Please amend paragraph [0017] as follows:

[0017] Transmitter- and receiver circuit parts 4a, 4b of circuit part 4 assigned to expansion unit 3 each have a semiconductor switch T1, T3, which may be an n-p-n switching transistor. In this connection, transmitter terminal Tx_Ew is connected via an ohmic resistance to the base of a transistor T3. The emitter of transistor T3 is connected to reference potential ground (GND) and connectable via reference potential line 8a to circuit part 2 assigned to basic unit 1. The collector of transmitter resistor T3 is connected, via a Zener diode D1 and a resistor R1 connected in series thereto, to the base of transistor T1 of receiver circuit part 4b and is moreover connected to power supply 6 for the purpose of current impression. Via the collector of transistor T3, moreover, circuit part 4, which is assigned to expansion unit 3, is connectable via data transmission line 8b to circuit part 2, which is assigned to basic unit 2. Receiver terminal Rx_Ew may include the collector of transistor T1, the collector being pulled to 5V via a pull-up resistor. The emitter of transistor T1 is connected to ground potential.

Please amend paragraph [0018] as follows:

[0018] Power supply 6 may include by a p-n-p transistor T2 which is connected on the emitter side to a supply potential (here 24 V) via an ohmic resistor R2, transistor T2, on the base side, being also connected to the supply potential via a Zener diode D2 as well as to the reference potential via a further ohmic resistor and, via its collector terminal, to data transmission line 8b.

Please amend paragraph [0020] as follows:

[0020] The base of transistor T2 is supplied via a voltage divider including a Zener diode D2 and a resistor, Zener diode D2 being connected to +24V on the cathode side and to ground potential via the resistor on the anode side.

Please amend paragraph [0021] as follows:

[0021] Transmitter- and receiver circuit parts 2a, 2b of circuit part 2 assigned to basic unit 1 may also built with semiconductor switches Opto1, Opto2. In the embodiment shown, these semiconductor switches are designed as circuit elements which ensure a galvanic separation, preferably as optocouplers Opto1, Opto2. Receiver circuit part 2b includes an optocoupler (Opto2) which is connected to ground potential via its emitter on the transistor side (with n-p-n transistor stage). The collector is connected to Vcc potential (here approximately 5V) via a pull-up resistor and, at the same time, is included in the receiver terminal RX_CPU on the side of the basic unit.

Please amend paragraph [0025] as follows:

[0025] In the rest state of the data transmission system, output transistors T3 or T_Opto1 (transistor of optocoupler Opto1) of the two transmitter circuit parts 2a, 4a, respectively, are blocked (collector-emitter path non-conducting). Impressed current Iq is divided between the two receiver circuit parts 2b, 4b. In this context, the data transmission system may be dimensioned in such a manner that the largest portion of the current flows through data transmission line 8b and through the receiver circuit part 2b (D3, D_Opto2 (diode of second optocoupler Opto2)) assigned to basic unit 1. In this manner, the susceptibility to failure of the circuit is minimized.

Please amend paragraph [0026] as follows:

[0026] In power supply 6, featuring Zener diode D2 and transistor T2, the current is:

$$Iq = V_{R2}/R2 = (V_{D2} - V_{EB\_T2})/R2$$

Please amend paragraph [0042] as follows:

[0042] In an embodiment of the present invention, transmitter- and receiver circuit parts (2a, 2b) are designed as elements which ensure a galvanic separation, and may be optocouplers (Opto1, Opto2). Transmitter- and receiver circuit parts (4a, 4b) may be designed in the form of transistor stages.